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Patentanmeldung Nr. | Patent application No. | Demande de brevet n°

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Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
p.o.

R C van Dijk

DEN HAAG, DEN
THE HAGUE, 29/01/02
LA HAYE, LE

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Blatt 2 der Bescheinigung
Sheet 2 of the certificate
Page 2 de l'attestation

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Method for testing an integrated circuit with a test device

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Method for testing an integrated circuit with a test device

Introduction

This document aims at presenting techniques for tester's resources reduction. Aiming at reducing the number of required resources can have several advantages such as reducing the test and tester cost, reducing the number of contacted pins or pads. Therefore, enabling multi site testing and/or reducing the effect of industrial problems such as bad contact yield loss[1]. The scope of this document is to present techniques that would reduce the number of required digital resources on a tester. It does not tackle the analogue world and therefore strictly focuses on digital techniques.

Two different techniques will first be presented, then, it will be explained in more detail how and when they should be implemented. Finally, a short case study will be given in order to evaluate the benefits and drawbacks of the such techniques when applied on a real device.

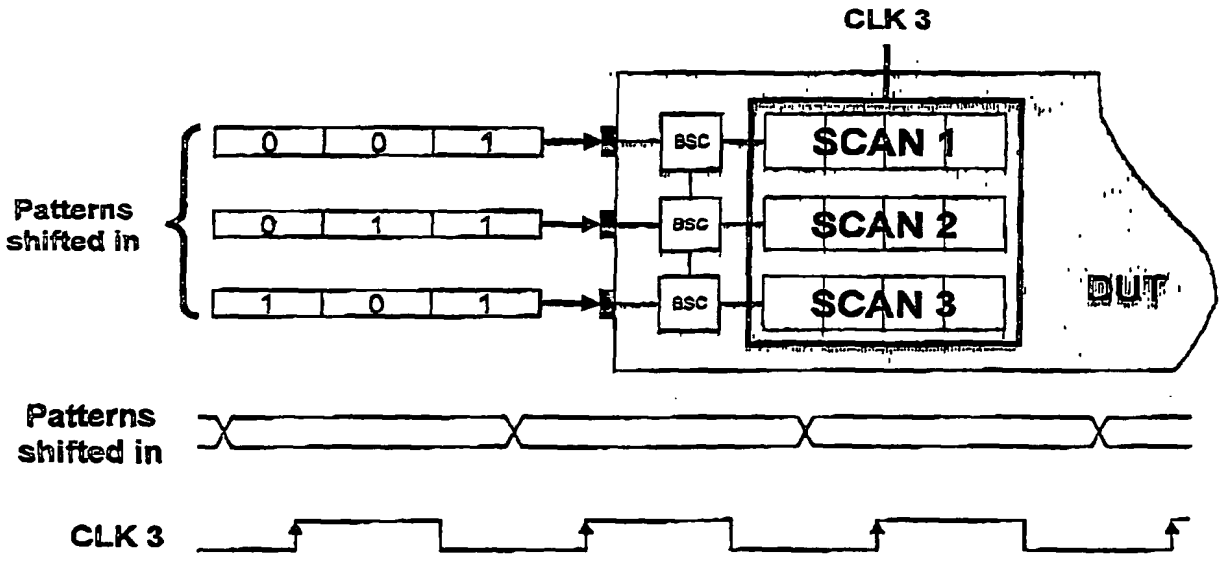
Scan test

Standard scan input principle

The scan input principle (shift in phase) is described by the following block and timing diagrams. It is quite a well known concept and we will therefore not concentrate to much on this part, for further information, refer to the Test Guidelines (version 2.0 or greater) [4] or to other related documentation.

Briefly, scan input consists of feeding logical values into specific shift registers (referred to as scan chains that can be several thousands bits long) and then of applying the content of those registers to the random logic in order to set it in specific states required for test purposes. The series of successive logical values are called patterns that are shifted in the scan chains.

Therefore, the patterns have to be applied to the scan chains inputs via a tester at the shift registers frequency (given in the following diagrams by CLK3 also called scan frequency).



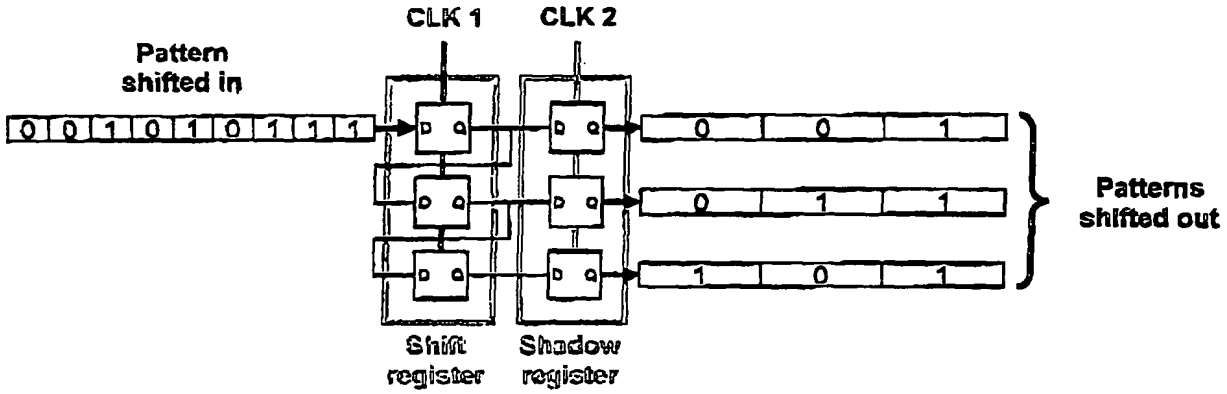
Principle of a three scan chains shift in phase

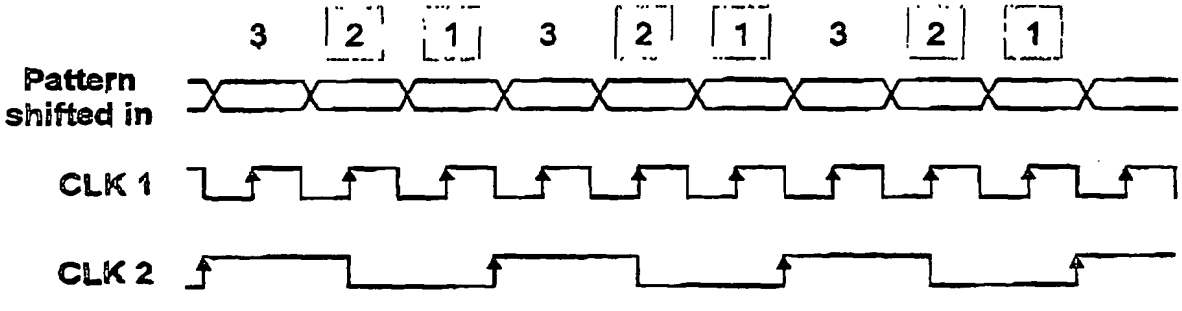
It is to notice that using this principle, a tester digital source running at the scan frequency is required for each scan chain input.

Note: In the previous block diagram, BSC (Boundary Scan Cells) are shown though not always present in front of scan chains. Whenever they are present, they behave as simple wires during scan test.

Shift register principle

It is quite obvious from the following block and timing diagrams to understand what a shift register does. On every CLK1 rising edge, the state of each flip-flop of the shift register is put on the flip-flop immediately following (i.e. from the top to the bottom). This is what is called the shift mode.
Then having access to each flip-flop output allows to perform a serial to parallel conversion or a time de-multiplexing.
In the following example the input bit stream is converted into three output bit streams. The latter are running at a frequency three time lower than the input bit stream frequency.



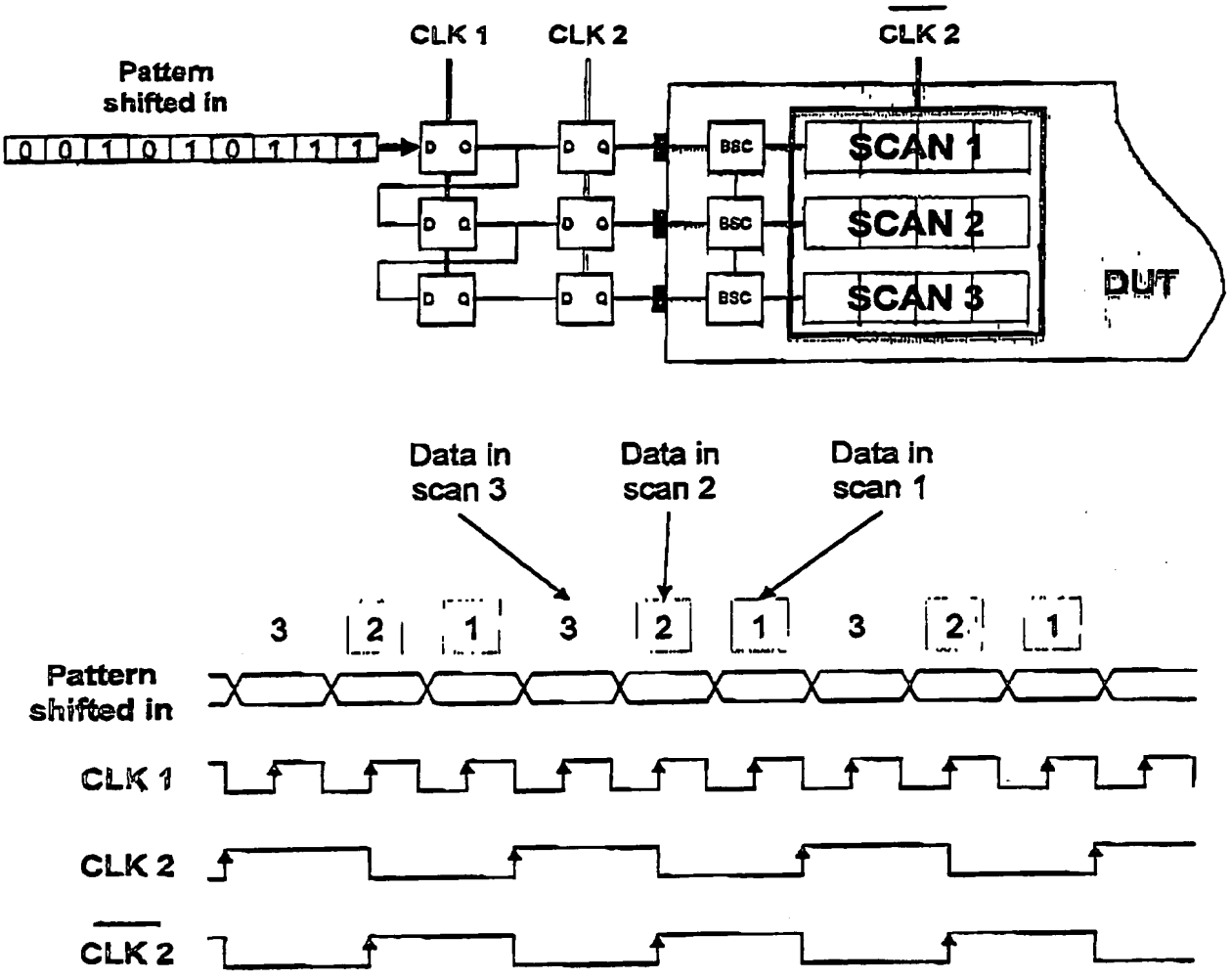


Three bits shift register principle

Readers may have noticed that the outputs of the shift register are buffered by a shadow register made with flip-flops. This shadow register is not mandatory, nevertheless it allows to get a stable output during shift mode. Indeed, the outputs remain unchanged between each rising edge of CLK2 signal.

Time multiplexed scan test input

As shown in the following block and timing diagrams, combining both scan input and shift register principles may allow to reduce the number of patterns needed for scan test (though these patterns are larger than the previous ones). Indeed, using a shift register allows to convert a time multiplexed serial pattern into several parallel scan patterns that can be applied to the device under test the same way they are in standard scan test.



Three multiplexed scan patterns input example

To be able to perform such a time multiplexed scan test, we must be able to generate the time multiplexed pattern shifted in, the CLK1 and the CLK2.
CLK2 need to run at the DUT scan frequency F_s, while the shifted in pattern and the CLK1 signal must run at n time F_s, where n is the width of the shift register. Of course, in this case, the length of the time multiplexed shifted in pattern is n time the length of the parallel scan patterns.

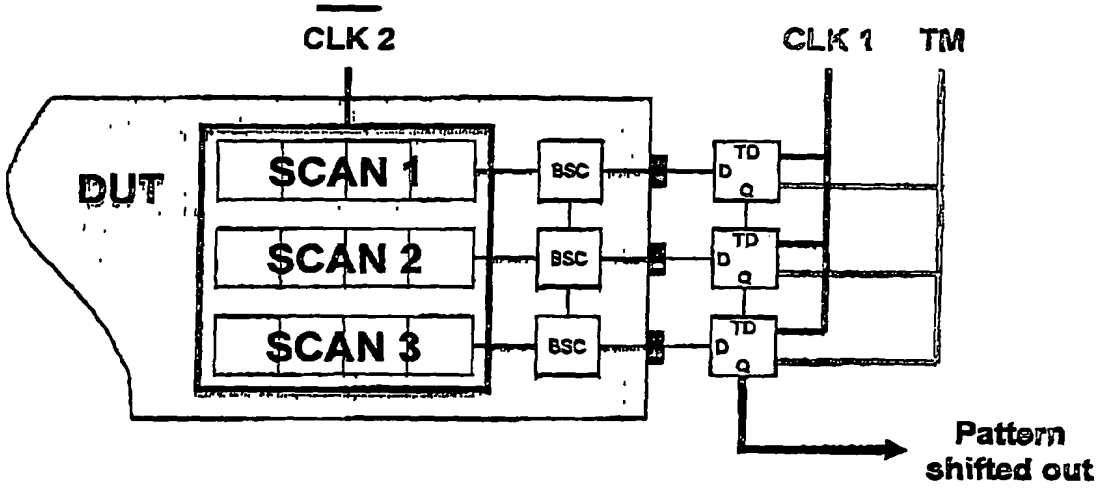
Time multiplexed scan test output

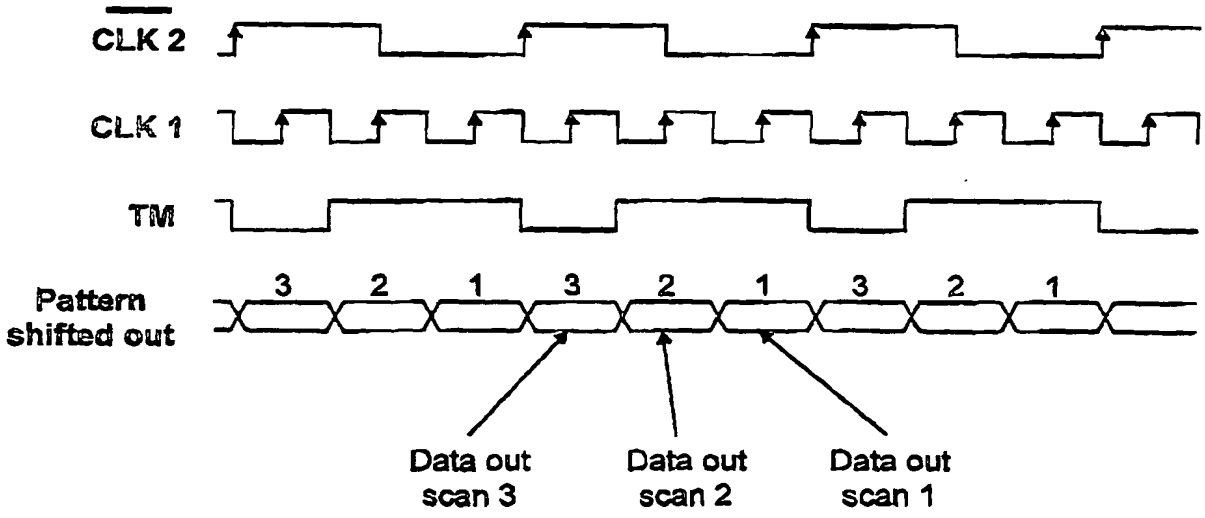
During standard scan test, patterns are shifted out at each scan chain output. Nevertheless, using the reciprocal principle to the previous one, i.e. performing a time multiplexing instead of a time de-multiplexing, may allow to reduce the number of output patterns.

This require to perform a parallel to serial conversion as shown in the following block and timing diagrams, that can be achieved using a scan chain. During normal mode (TM signal low) data acquisition is performed at the DUT outputs, and during shift mode (TM signal high) data is transferred from a scan flip-flop to the following one.

To be able to apply this principle, we must be able to generate CLK1 and TM signals and to acquire the time multiplexed pattern shifted out.

CLK1 and TM signals must run at n time F_s, where n is the length of the scan chain and F_s the DUT scan frequency. The same way, the pattern shifted out must be acquired at n time F_s.





Three multiplexed scan patterns output example

Tester point of view

From a tester point of view, assuming that L is the vector length (i.e. summation of all needed patterns length), F_s the standard shift frequency and n the shift register width or output scan chain length. The tester requirements are given by the following relations.

$$F_{max} \geq n \times F_s \qquad (1)$$

and

$$Mem_{width} \geq n \times L \qquad (2)$$

Where F_{max} stands for the tester digital channel maximum frequency and Mem_{width} stands for the tester available memory per digital channel.
Therefore, n can be determined using the following equation.

$$n = Int\left(min\left(\frac{F_{max}}{F_s}, \frac{Mem_{width}}{L} \right) \right) \qquad (3)$$

It is to notice that the previous formula assumes that both the shift register and the output scan chain are able to support frequencies higher or equal to F_{max}. Whenever it is not the case, this has to be taken into account in the formula replacing F_{max} by the lowest frequency in order to determine a relevant n value.
Then the number of digital channels required for scan test data generation and acquisition is given by the following:

$$N_{dig} = 2 \times Int\left(\frac{n_{scan} - 1}{n} \right) + 2 + CLK1 + CLK2 + TM \qquad (4)$$

Where N_{dig} and n_{scan} stand for the number of required digital channels and the number of scan chains respectively and CLK1, CLK2 and TM refer to signals shown in previous diagrams.
This has to be compared to $2 \times n_{scan}$ which is the number of required digital channels for standard scan test.

In the following example, let's assume that the device to be tested contains 80 scan chains, that the standard scan test shift frequency F_s is 10Mhz and that the vector memory required for L is 1Meg.
On the other hand, let's assume that the tester digital channel maximum frequency F_{max} is 50Mhz and that the available memory per digital channel Mem_{width} is 4Meg.
Applying relation (3) allows to determine the width of the input shift register and the length of output scan chain and gives

$$n = 4$$

Then, applying relation (4) gives the number of required digital channels.

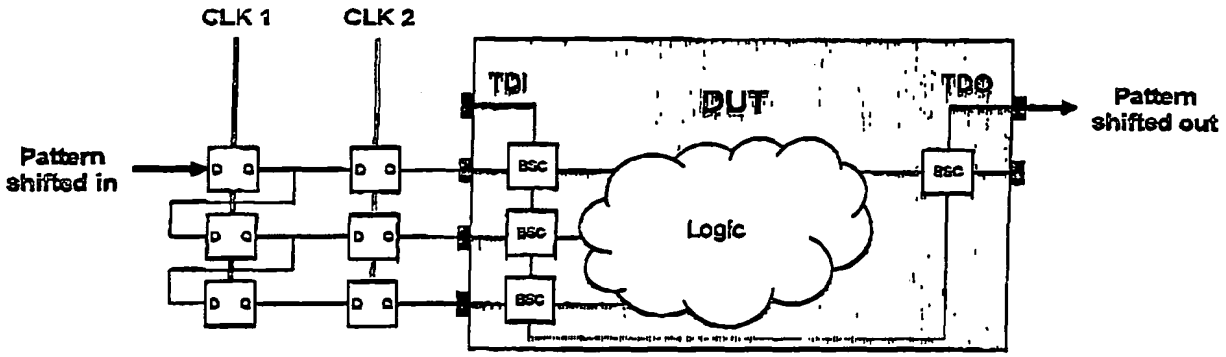
$$N_{dig} = 43$$

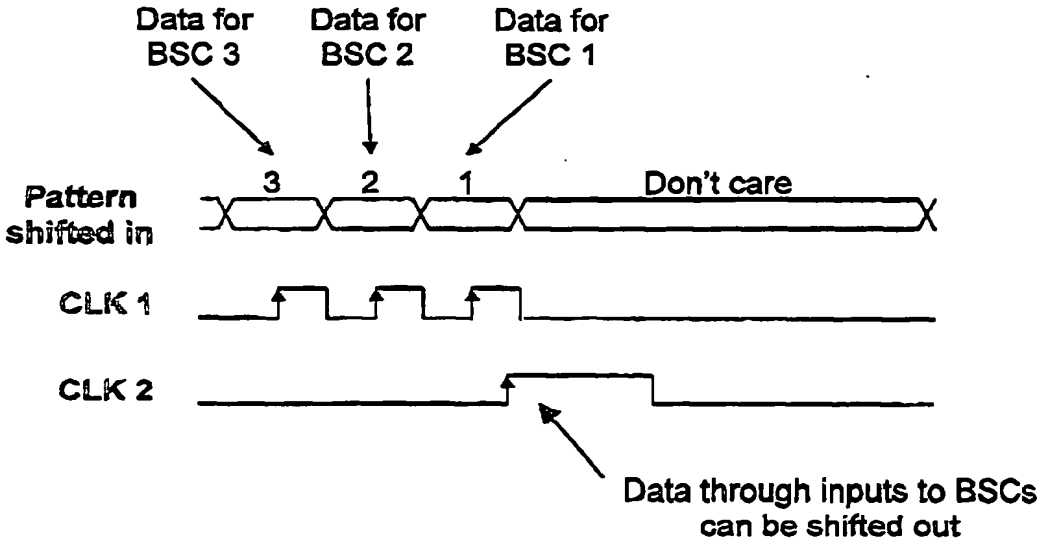
This has to be compared to 160 required digital channels for standard scan test. Which makes an absolute reduction of 116 digital channels or a relative reduction of 72.5%. This example clearly shows that applying such a time multiplexed scan test has a significant impact on the number of required tester digital channels.

Time multiplexed boundary scan test

Time multiplexed boundary scan input

Using the same kind of shift register as the one previously presented for scan test may allow to test for continuity between input boundary scan cells (BSCs) and pads or pin depending on whether the test is performed at wafer level or at packaged device level.
Indeed, as shown in the following block and timing diagrams, using a shift register of length equal to the number of input BSCs and connecting all shift register outputs to a BSC's input, via a shadow register, allows to apply any logical level at the BSC's inputs.
The data applied on the BSCs can then be acquired by the BSCs, shifted out via the standard TDO pin and be compared to expected values in order to determine whether any opens/shorts are presents.
There are no frequency constraints for CLK1 and CLK2 signals, though the faster they are running the faster will be the test. Nevertheless, as the number of BSC's inputs to test is not very large (few hundreds of inputs), even with relatively low shift in frequency (CLK1), the test time will remain very short.





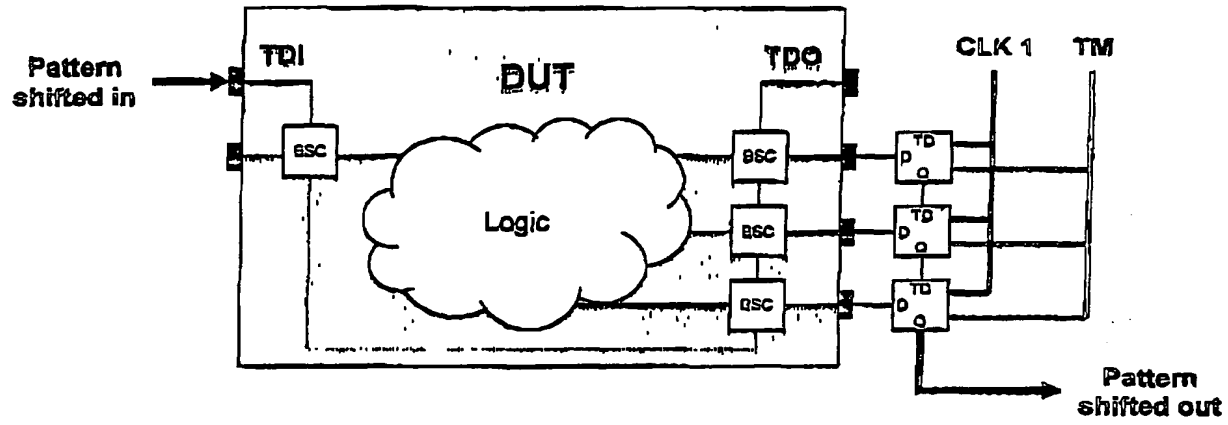
Three inputs BSCs example

Time multiplexed boundary scan output

The same strategy can be applied to test for continuity between output BSCs and pad or pin depending on whether the test is performed at wafer level or at packaged device level. Indeed, as shown in the following block and timing diagrams, each output BSC can be connected to the inputs of a scan chain of length equal to the number of output BSCs, the same way it was for time multiplexed scan test output.

Therefore, data can be shifted through the standard TDI input in order to load output BSCs with logical values. Those values are acquired by the scan chain during a normal mode cycle (TM signal low), then shifted out during shift mode cycles (TM signal high) and finally compared with to expected values in order to determine whether any opens/shorts are presents.

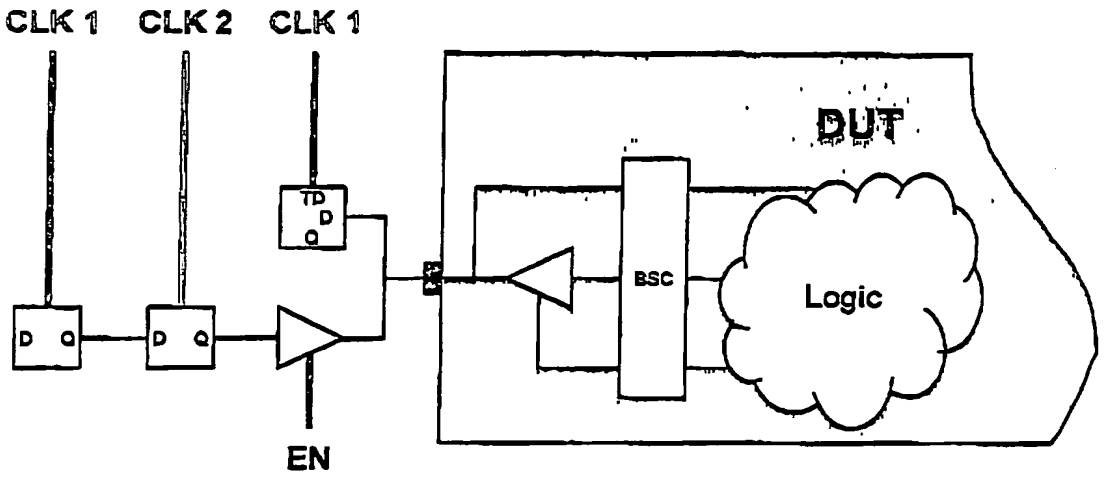
Again, there are no frequency constraints for CLK1 and TM signals, though the faster they are running the faster will be the test. Nevertheless, as the number of BSC's outputs to test is not very large (few hundreds of outputs), even with relatively low shift out frequency (CLK1), the test time will remain very short.



Three outputs BSCs example

Time multiplexed boundary scan input/output

There may be Input / Output BSCs in the device. Whenever it happens, a combination of the two previous principle is required to fully test for continuity. It is quite straight forward to combine the input/output principles, nevertheless, there need to be a tri-state buffer added in order to make sure that both tester and DUT will not drive conflicting values at the same time. The remaining parts are exactly the same as the previously explained one and will therefore not be explained in more details.



Input/output boundary scan cell test structure example

Tester point of view

From a tester point of view, in order to perform such a boundary scan test approach, it is needed to be able to generate CLK1, CLK2, EN and TM signals. There is also the need for two digital resources in order to apply the pattern at the shift register input and in order to acquire the pattern at the scan chain output. Shifted in pattern through TDI and shifted out pattern through TDO require TDI and TDO to be connected to a digital resources, but as those two pins are already connected in standard test, they are not considered as extra required resources.
Therefore, the number of digital resources needed for this approach is 4.
This as to be compared to the number of pins or pads that have to be contacted in order to test for continuity. This is purely device dependant, nevertheless, the reduction in terms of number of resources can be quite significant.

Implementation

Time multiplexed scan test can be implemented on both test board and chip. The only requirement is that both input shift registers and output scan chains can support the required clock frequency (a multiple of the device scan clock frequency).
This technique has the advantage to be applicable for both wafer and final tests. Also, as demonstrated in paragraph 1.5, it can significantly reduce the number of required digital resources.
When it is implemented on board, it does not reduce the number of contacted pads or pins. Therefore, at wafer test level, the number of probes is not reduced and then the industrialisation problems due to high number of contacted pads are not lessened. For this reason, it is preferred to implement this techniques on chip during the design phase as a DfT feature.
When it is done this way, the number of contacted pads during wafer test is reduced. Thus, there are less needles on probe cards which result in less industrialisation problems. Of course, implementing this DfT technique on chip adds extra area to the device. Nevertheless, it does just require four extra flip-flops per scan chains. As an example, for a 100 scan chains device, it just adds 400 flip-flops, which is almost insignificant with respect to the overall device area.

Test patterns have to be generated using the usual CAT tools. It is then needed to time multiplex them according to the device test implementation.

Time multiplexed boundary scan test should not be implemented on the device since then it would not allow to test all continuities between boundary scan cells and pads or pins but only between the contacted pad or pin and the corresponding boundary scan cell. Then, this technique should only be implemented on board.
The consequence of this is that it will not reduce the number of needles per probe cards. Therefore, it is preferable to apply this technique at final test level. For wafer test, it is recommended to use such techniques as I/O wrap [3] that need to be implemented on chip during the design phase. Nevertheless, when such features are not present, it still remains a good alternative to use time multiplexed boundary scan test at wafer test in order to reduce number of required resources.
Specific patterns have to be generated in order to test continuities. There may be plenty of different patterns such as alternative zero and one and complementary or such as walking one and walking zero. It is up to the DfT and test engineers to decide which strategy they will apply.

SAA7215 case study

This paragraph aims at determining roughly what would the presented LCT approach give when applied to the SAA7215 device at wafer test level.
Performed tests on this device at wafer test are

- Consumption
- Leakage
- Opens / shorts
- Scan continuity
- Stuck at fault
- Memories
  - BIST
  - Scan access

With the proposed techniques, all tests can be performed except from leakage tests since they require some parametrical measurements[1]. Those tests are also performed during final test, there would therefore not be any critical risks with respect to PPM level. The only drawback is due to the faulty packaged devices extra cost, taking into account that about 2% of devices fail the leakage tests during wafer test.

This device contains 76 scan chains running at 6.75Mhz. Applying relation (3) with no constraint on vector memory depth and with a maximum digital resource frequency Fmax equal to 30Mhz gives a shift register width n equal to 4.
Then applying relation (4) gives a number of 41 required digital resources in order to perform multiplexed scan test.

[1] It is to notice that the proposed time multiplexed boundary scan techniques does not allow to perform parametrical measurements. Several techniques such as one using relay switch matrix exist that have been presented in literature [2] and that allow to test for opens/shorts and to perform parametrical measurements on all pins. The drawback of those techniques is that all pin cannot be tested in parallel but sequentially resulting in longer test time. Therefore, selecting one technique among all existing ones has to be made taking into account the compromise between test coverage and test time.

Extra digital resources are required to directly contact some device's pads. Namely the JTAG interface with TCK, TDI, TMS, TRST and TDO signals plus three specific resources for CP81MEXT, CLK_BUS and FSCLK pads. This makes a total amount of 8 extra digital resources.

Then, 4 digital resources may be needed to contact all remaining digital pins using time multiplexed boundary scan technique.
Also, a high speed clock signal is required.

This makes a total amount of 53 digital resources plus 1 high speed clock.

Finally, there are around 15 supply pads and 15 ground pads.

Therefore, the probe card needed to perform such a test would be a 84 needles probe card. This has to be compared to the around 220 needles actual probe card. Such a reduced needles probe card would of course reduce the industrialisation problems and may allow to perform multi site testing.

References

[1] Low Cost Tester Strategy - J. Santiago - Version 1.0 draft
[2] Limited Pin Test Design Guidelines - Version 1.1a - November 10, 1999
[3] Reduced Pin Count and I/O Wrap Test - H. Vranken - Draft version - June 2000
[4] Test Guidelines - D. Lelouvier - P. Poirier - Version 2.0 - June 2000

CLAIMS

1. Method for testing an integrated circuit with a test device, said circuit comprising a first pin and a second pin, a first internal scan chain and a second internal scan chain, said method comprising the following steps:
   - receiving a first data element and a second data element in a serial fashion;
   - feeding the first data element to the first scan chain through the first pin and feeding the second data element to the second scan chain through the second pin in a parallel fashion.